REMARKS

The Examiner is thanked for the performance of a thorough search. By this amendment, Claims 1, 3, 10, 18, 22, 24, 26, 29 and 31 have been amended and new Claim 34 has been added. Hence, Claims 1-34 are pending in this application. The amendments to the claims and new Claim 34 do not add any new matter to this application. All issues raised in the Office Action mailed August 16, 2000 are addressed hereinafter.

REJECTION OF CLAIM 10 UNDER 35 U.S.C. §112, SECOND PARAGRAPH

Claim 10 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The stated basis for this rejection is that it is unclear what is being determined in the determining step.

Claim 10 has been amended to correct a typographical error that Applicant believes caused the confusion. Specifically, the amendment clarifies that "the routing path between the first and second integrated circuit devices" is what is being determined in the determining step. Furthermore, in Claim 10, the routing path "is routed from the second integrated circuit device to the first integrated circuit device."

In view of the amendment to Claim 10, it is respectfully submitted that Claim 10, as amended, particularly points out and distinctly claims the subject matter that Applicant regards as the invention. Accordingly, reconsideration and withdrawal of the rejection of Claim 10 under 35 U.S.C. §112, second paragraph is respectfully requested.

REJECTION OF CLAIMS 1-5, 10, 15 AND 22-33 UNDER 35 U.S.C. §102(b)

Claims 1-5, 10, 15 and 22-33 were rejected under 35 U.S.C. §102(b) as being unpatentable over *An Interactive Maze Router with Hints*, by Michael H. Arnold and Walter S. Scott ("*Arnold*"). It is respectfully submitted that Claims 1-5, 10, 15 and 22-33, as amended, are not anticipated by *Arnold* for at least the reasons provided hereinafter.

CLAIM 1

Claim 1, as amended, recites a method for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located to connect first and second integrated circuit devices from the set of two or more integrated circuit devices;
> determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices."

Claim 1 addresses the problem of how to automatically route an integrated circuit while avoiding problems appurtenant to conventional automated routing approaches.

Arnold discloses an interactive maze router that uses fence and magnet hints. Fence boundaries designate regions where routing is allowed, or regions where routing is prohibited. Magnets "pull" routing in a particular direction, typically to cause routing to

hug one side of a routing region (See, for example, *Arnold*, at page 673, Section 2, third paragraph).

It is respectfully submitted that *Arnold* does not anticipate amended Claim 1 because *Arnold* does not in any way teach or suggest at least several of the steps required by amended Claim 1. Claim 1, as amended, requires the step of "determining, based upon the integrated circuit layout data and the integrated circuit connection data, **a set of one or more routing indicators that specify a set of one or more preferable intermediate routing locations through which a routing path is to be located** to connect first and second integrated circuit devices from the set of two or more integrated circuit devices." Amended Claim 1 also requires the step of "determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path satisfies specified design criteria."

Neither of these required steps is in any way taught or suggested by *Arnold*. In particular, neither the fence boundaries, nor the magnets of *Arnold* constitute routing indicators that "**specify a set of one or more preferable intermediate routing locations through which a routing path is to be located.**" The fence boundaries of *Arnold* merely designate general regions where routing is allowed or prohibited. The magnets of *Arnold* merely influence the direction of routing and tend to pull routing to one side of a routing region. In *Arnold*, there is no determination of intermediate routing locations or points of any kind. Furthermore, the fence boundaries and magnets of *Arnold* are global indicators that are not specific to a particular routing path.

The approach recited in amended Claim 1 provides the advantage that the routing path can be routed along the intermediate routing locations specified by the routing indicators without having to make further routing placement decisions. This advantage cannot be realized by the approach described in *Arnold* since, even after the fences and magnets are established, the decision about where to route a connection within the allowable routing regions must still be made.

For at least these reasons, it is respectfully submitted that amended Claim 1 is not in any way taught or suggested by *Arnold* and that Claim 1 is therefore not anticipated by *Arnold*.

CLAIMS 2-5, 10 AND 15

Claims 2-5, 10 and 15 depend on Claim 1 and include all of the limitations of Claim 1. Accordingly, it is respectfully submitted that Claims 2-5, 10 and 15 are not anticipated by *Arnold* for at least the reasons provided herein with respect to Claim 1. Furthermore, it is respectfully submitted that Claims 2-5, 10 and 15 recite additional limitations that independently render them patentable over *Arnold*.

For example, Claim 3 requires the additional steps of:

> "identifying one or more obstacles that block the routing path,
> determining, based upon the integrated circuit layout data, the integrated circuit connection data and the one or more obstacles, one or more additional routing indicators that specify one or more preferable routing locations through which the routing path is to be located to avoid the one or more obstacles, and
> determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more additional routing indicators, the routing path between the first and second integrated circuit devices."

Claim 3 addresses the problem of how to route an integrated circuit when the layout may contain obstacles. According to Claim 3, obstacle avoidance is performed by identifying obstacles that block the routing path and determining additional routing indicators that specify "preferable routing locations through which the routing path is to be located to avoid the one or more obstacles." *Arnold* describes factoring major obstacles into global cost estimation using a cost estimation plane containing only large-scale obstacles (subcells and fences). Global cost estimation is used to estimate the cost of completing partial paths. Thus, the approach described in *Arnold* attempts to reduce extending paths that are headed in the wrong direction by including large obstacles in the cost estimate. *Arnold*, however, does not teach or suggest determining additional routing indicators that "specify preferable routing locations through which the routing path is to be located to avoid the one or more obstacles," as is required by amended Claim 3. For at least these reasons, it is respectfully submitted that amended Claim 3 is not in any way taught or suggested by *Arnold* and that Claim 3 is therefore not anticipated by *Arnold.*

As another example, Claim 10 requires the additional steps of:

> "identifying one or more obstacles that block the routing path, and
> determining, based upon the integrated circuit layout data, the integrated circuit connection data and the set of one or more routing indicators, the routing path between the first and second integrated circuit devices, wherein the routing path is routed from the second integrated circuit device to the first integrated circuit device."

Claim 10 addresses the problem of how to route an integrated circuit when the layout may contain obstacles. According to Claim 10, obstacle avoidance is performed by routing from the second integrated circuit device to the first integrated circuit device. This approach is not taught or suggested by *Arnold. Arnold* discloses using "distance to the goal" to identify paths that are entirely headed in the wrong direction. This approach

however, is performed with respect to the starting location. *Arnold* does not in any way teach or suggest routing backwards from the destination to the source to avoid obstacles. For at least these reasons, it is respectfully submitted that amended Claim 10 is not in any way taught or suggested by *Arnold* and is therefore not anticipated by *Arnold.*

CLAIM 22

Claim 22, as amended, recites a method for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a set of two or more join points that are to be electrically connected, wherein each join point from the set of two or more join points has an associated set of specified design criteria that control attachment of routing paths thereto;
> determining, based upon the integrated circuit layout data and the set of two or more join points, one or more routing paths to connect the set of two or more join points, wherein the one or more routing paths satisfy the specified design criteria associated with the set of two or more join points; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the one or more routing paths."

Claim 22, as amended, recites an approach for automatically routing an integrated circuit that requires the use of join point-specific design criteria to control the attachment of routing paths to join points. Using join point-specific design criteria allows relatively greater flexibility than conventional approaches that use global design criteria. For

example, using join point-specific design criteria allows design rules to be selectively applied to join points and not to, for example, routing paths, other layout features or other join points.

The approach disclosed in *Arnold* uses a global cost function to identify the most preferable paths, or at least to discontinue paths that are headed in completely the wrong direction. *Arnold* does not in any way teach or suggest using join point-specific design criteria to automatically route an integrated circuit.

For at least these reasons, it is respectfully submitted that Claim 22, as amended, is not in any way taught or suggested by *Arnold* and is therefore not anticipated by *Arnold.*

CLAIM 23

Claims 23 recites a method for automatically routing an integrated circuit that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more integrated circuit devices to be included in the integrated circuit;
> receiving integrated circuit connection data that specifies one or more electrical connections to be made between the integrated circuit devices;
> determining, based upon the integrated circuit layout data and the integrated circuit connection data, a routing path between first and second integrated circuit devices that satisfies specified design criteria, wherein determining the routing path between the first and second integrated circuit devices includes
> determining whether the distance to be routed for a portion of the routing path exceeds a specified distance, and
> if the distance to be routed for the portion of the routing path does not exceed the specified distance, then routing the portion of the routing path in a single step; and
> updating the integrated circuit layout data to generate updated integrated circuit layout data that reflects the routing path between the first and second integrated circuit devices."

The approach recited in Claim 23 requires that a portion of a routing path be extended in a single step by an amount that does not exceed a specified distance. This approach is particularly useful in tight routing situations where the distance to be routed is so short that independent bends cannot be made, the selection of connection locales impacts the feasibility of routing or the remaining unrouted stretch after moving out from a join point is too short to add bends. In addition, construction of an entire feasible route in a single step allows error recovery mechanisms to make better decisions as to what should be removed. Otherwise, the recovery mechanism may have only short routing stubs as guidance.

The approach recited in *Arnold* uses a conventional cost function to select a particular routing. *Arnold*, however, does not teach or suggest routing an integrating circuit by extending in a single step, a portion of a route by an amount that does not exceed a specified distance.

For at least these reasons, it is respectfully submitted that Claim 23 is not anticipated by *Arnold* and is therefore patentable over *Arnold*.

CLAIMS 24-28

Claims 24-28 recite limitations similar to Claims 1-5, except in the context of a computer-readable medium. It is therefore respectfully submitted that Claims 24-28 are not anticipated for at least the reasons set forth herein with respect to Claims 1-5.

CLAIMS 29-33

Claims 29-33 recite limitations similar to Claims 1-5, except in the context of a computer system. It is therefore respectfully submitted that Claims 29-33 are not anticipated for at least the reasons set forth herein with respect to Claims 1-5.

In view of the foregoing, reconsideration and withdrawal of the rejection of Claims 1-5, 10, 15 and 22-33 under 35 U.S.C. §102(b) as being anticipated by *Arnold* is respectfully requested.

REJECTION OF CLAIM 21 UNDER 35 U.S.C. §102(b)

Claim 21 was rejected under 35 U.S.C. §102(b) as being anticipated by *A Practical Online Design Rule Checking System*, by Goro Suzuki and Yoshio Okamura ("*Suzuki*"). It is respectfully submitted that Claim 21 is not anticipated by *Suzuki* for at least the reasons provided hereinafter.

Claim 21 recites a method for automatically verifying an integrated circuit layout that requires the steps of:

> "receiving integrated circuit layout data that defines a set of two or more layout objects contained in the integrated circuit layout;
> performing a first design rule check on a layout object from the set of two or more layout objects by evaluating the layout object against specified design criteria;
> changing one or more values defined by the specified design criteria to generate updated specified design criteria, wherein the changing of the one or more values is performed after a specified amount of time has elapsed and is made with respect to either the layout object or one or more other layout objects from the set of two or more layout objects; and
> performing a second design rule check on the layout object by evaluating the layout object against the updated specified design criteria."

Claim 21 recites a time-varying design rule check approach for verifying an integrated circuit layout. One or more values defined by specified design criteria used for a design rule check are varied over time with respect to one or more layout objects

contained in the integrated circuit layout. *Suzuki* discloses a conventional incremental design rule checking system that selectively applies all or a portion of a set of design rule checks to portions of an integrated circuit layout. *Suzuki*, however, does not in any way teach or suggest the time-varying design rule check approach recited in Claim 21. The Examiner is invited to identify specific portions of *Suzuki* that disclose the approach recited in Claim 21.

For at least these reasons, it is respectfully submitted that Claim 21 is not anticipated by *Suzuki* and is therefore patentable over *Suzuki*. Accordingly, reconsideration and withdrawal of the rejection of Claim 21 under 35 U.S.C. §102(b) as being anticipated by *Suzuki* is respectfully requested.

REJECTION OF CLAIMS 6-9 AND 12 UNDER 35 U.S.C. §103(a)

Claims 6-9 and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Arnold* and *Codar: A Congestion-Directed General Area Router*, by Ping-San Tzeng and Carlo H. Sequin ("*Tzeng*"). It is respectfully submitted that Claim 21 is patentable over *Arnold* and *Tzeng*, alone or in combination, for at least the reasons provided hereinafter.

Claims 6-9 and 12 depend on Claim 1 and include all of the limitations of Claim 1. *Tzeng* is relied upon for its disclosure of rip-up and reroute techniques that are not taught or suggested by *Arnold*. *Tzeng*, however, does not in any way teach or suggest an approach for automatically routing and integrated circuit using routing indicators that "specify a set of one or more preferable intermediate routing locations through which a routing path is to be located" as is required by Claims 6-9 and 12.

Accordingly, for this reason and the reasons set forth herein with respect to Claim 1, it is respectfully submitted that Claims 6-9 and 12 are not in any way taught or suggested by *Arnold* and *Tzeng*, alone or in combination. Reconsideration and withdrawal of the rejection of Claims 6-9 and 12 under 35 U.S.C. §103(a) as being unpatentable over *Arnold* and *Tzeng* is therefore respectfully requested.

REJECTION OF CLAIMS 11, 13, 14 AND 16-20 UNDER 35 U.S.C. §103(a)

Claims 11, 13, 14 and 16-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Arnold* in view of *An Interactive Router for Analog IC Design*, by Thorsten Adler and Jurgen Scheible ("*Adler*"). It is respectfully submitted that Claims 11, 13, 14 and 16-20 are patentable over *Arnold* and *Adler*, alone or in combination, for at least the reasons provided hereinafter.

CLAIM 11

Claim 11 depends from Claim 1 and includes all of the limitations of Claim 1. Claim 11 further requires the steps of:

> "identifying one or more obstacles that block the routing path,
> determining one or more locations to employ corner clipping to provide additional space for routing the routing path, and
> determining, based upon the integrated circuit layout data, the integrated circuit connection data, the set of one or more routing indicators and the one or more locations to employ corner clipping, the routing path between the first and second integrated circuit devices."

Claim 11 requires employing corner clipping to provide additional space for a routing path to avoid obstacles. It is respectfully submitted that *Adler* does not in any way teach or suggest an approach for automatically routing an integrated circuit that employs corner clipping to avoid obstacles, as required by Claim 11. *Adler* suggests

using non-orthogonal routing to reduce wire length when routing around the corner of an obstacle, but does not suggest actually clipping the corner of an obstacle to provide additional space for a routing path. The Office Action states that "The *Adler* paper teaches global and maze routing which suggests corner clipping." The Examiner is invited to cite specific portions of *Adler* that teach or suggest corner clipping.

For at least these reasons, it is respectfully submitted that Claim 11 is not in any way taught or suggested by *Arnold* and *Adler*, alone or in combination, and that Claim 11 is therefore patentable over *Arnold* and *Adler*, alone or in combination.

CLAIMS 13 AND 14

Claims 13 and 14 depend from Claim 1 and include all of the limitations of Claim 1. It is respectfully submitted that *Adler* does not teach or suggest an approach for automatically routing and integrated circuit using routing indicators that "specify a set of one or more preferable intermediate routing locations through which a routing path is to be located" as is required by Claims 13 and 14. Accordingly, for this reason and the reasons set forth herein with respect to Claim 1, it is respectfully submitted that Claims 13 and 14 are not in any way taught or suggested by *Arnold* and *Adler*, alone or in combination, and that Claims 13 and 14 are therefore patentable over *Arnold* and *Adler*, alone or in combination.

CLAIMS 16-18

Claims 16-18 depend from Claim 1 and include all of the limitations of Claim 1. Claims 16-18 all require on-the-fly design rule checks on specific portions of geometry. Specifically, Claim 16 requires performing the step of determining the routing path

between the first and second integrated circuit devices by "performing one or more design rule checks on one or more portions of the routing path as the routing path is being determined." Thus, an on-the-fly design rule check is performed **as the routing path is being determined**. Claim 17 depends from Claim 16 and further requires "performing a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path." Thus, Claim 17 requires the on-the-fly design rule checking of Claim 16, selectively applied to exclude one or more layout objects previously checked during the determination of the routing path. Claim 18 requires selectively performing a design rule check on only an extended portion of a routing path.

It is respectfully submitted that *Arnold* and *Adler*, alone or in combination, do not in any way teach or suggest the on-the-fly design rule checking required by Claims 16-18 and that Claims 16-18 are therefore patentable over *Arnold* and *Adler*, alone or in combination. The Examiner is invited to cite specific portions of either reference that in any way teach or suggest the specific limitations required by Claims 16-18.

CLAIMS 19 AND 20

Claims 19 and 20 depend from Claim 1 and include all of the limitations of Claim 1. Claims 19 and 20 further require that attachment and bend angles defined by the updated integrated circuit layout geometry are orthogonal and non-orthogonal, respectively. Although *Adler* may teach or suggest using non-orthogonal geometry generally, *Adler* does not teach or suggest an approach for automatically routing and

integrated circuit using routing indicators that "specify a set of one or more preferable intermediate routing locations through which a routing path is to be located" as is required by Claims 19 and 20. Accordingly, for this reason and the reasons set forth herein with respect to Claim 1, it is respectfully submitted that Claims 19 and 20 are not in any way taught or suggested by *Arnold* and *Adler*, alone or in combination, and that Claims 19 and 20 are patentable over *Arnold* and *Adler*, alone or in combination.

In view of the foregoing, reconsideration and withdrawal of the rejection of Claims 11, 13, 14 and 16-20 under 35 U.S.C. §103(a) as being unpatentable over *Arnold* in view of *Adler* is respectfully requested.

REJECTION OF CLAIMS 16-18 UNDER 35 U.S.C. §103(a)

Claims 16-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Arnold* in view of *Suzuki*. It is respectfully submitted that Claims 16-18 are patentable over *Arnold* and *Suzuki*, alone or in combination, for at least the reasons provided hereinafter.

Claims 16-18 depend from Claim 1 and include all of the limitations recited in Claim 1. *Suzuki* does in any way teach or suggest an approach for automatically routing and integrated circuit using routing indicators that "specify a set of one or more preferable intermediate routing locations through which a routing path is to be located" as is required by Claims 16-18. Furthermore, *Arnold* and *Suzuki*, alone or in combination, do not in any way teach or suggest the on-the-fly design rule checks performed on specific portions of geometry as required by Claims 16-18. Specifically, Claim 16 requires performing the step of determining the routing path between the first and second integrated circuit devices by "performing one or more design rule checks on one or more

portions of the routing path as the routing path is being determined." Thus, an on-the-fly design rule check is performed **as the routing path is being determined**. Claim 17 depends from Claim 16 and further requires "performing a design rule check on the updated integrated circuit layout data, wherein the design rule check does not check one or more layout objects previously checked during determination of the routing path." Thus, Claim 17 requires the on-the-fly design rule checking of Claim 16, selectively applied to exclude one or more layout objects previously checked during the determination of the routing path. Claim 18 requires selectively performing a design rule check on only an extended portion of a routing path. The Examiner is invited to cite specific portions of *Suzuki* that teach or suggest these limitations.

For at least these reasons and the reasons set forth herein with respect to Claim 1, it is respectfully submitted that Claims 16-18 are not in any way taught or suggested by *Arnold* and *Suzuki*, alone or in combination. Accordingly, reconsideration and withdrawal of the rejection of Claims 16-18 under 35 U.S.C. §103(a) as being unpatentable over *Arnold* and *Suzuki* is therefore respectfully requested.

For the reasons set forth herein, it is respectfully submitted that all of the pending claims are in condition for allowance and the issuance of a notice of allowance is respectfully requested.

If there are any additional charges, please charge them to Deposit Account No. 50-1302.

Respectfully submitted,

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